What is claimed is:

1. A multi-port memory device, comprising:

a plurality of banks arranged at an upper and a lower portion of a core area as many as a fixed number in a row direction;

a multiplicity of ports located at edges of the upper and the lower portions of the core area, wherein respective ports perform independent communication with respective different target devices;

a first global data bus, located in a row direction between the ports and the banks arranged at the upper portion of the core area, for performing the parallel data transmission;

a second global data bus, located in a row direction between the ports and the banks arranged at the lower portion of the core area, for performing the parallel data transmission;

a plurality of local data buses, arranged in a column direction of each bank, for executing data transmission within the banks; and

a majority of local data bus connection units, located between two banks adjacent to each other in a column direction, for selectively connecting the local data buses corresponding to the two adjacent banks.

2. The multi-port memory device as recited in claim 1,

further comprising a control block arranged at one side of the core area.

3. A multi-port memory device, comprising:

a plurality of banks arranged at each of 4 quadrants obtained by dividing a core area in four as many as a fixed number in a row direction, wherein each bank includes a multiplicity of memory cells and a row decoder;

a majority of ports located at edges of said each of the 4 quadrants, wherein respective ports perform independent communication with respective different target devices;

a first to a fourth global data bus, located in a row direction between the ports and the banks corresponding to said each of the 4 quadrants, for performing the parallel data transmission;

a first and a second global data bus connection means, located between two global data buses adjacent to each other in a row direction, for selectively connecting the two global data buses;

a multiplicity of local data buses, arranged in a column direction of each bank, for executing data transmission within the banks; and

local data bus connection means, located between two banks adjacent to each other in a column direction, for selectively connecting local data buses corresponding to the two adjacent banks.

4. The multi-port memory device as recited in claim 3, further comprising a control block arranged between the first and the third quadrants and the second and the fourth quadrants to divide the core area in two.

5. A multi-port memory device, comprising:

a plurality of banks arranged at each of 4 quadrants obtained by dividing a core area in four as many as a fixed number in a row direction, wherein each bank includes a multiplicity of memory cells and a row decoder;

an intermediating means, located between the first and the third quadrants and the second and the fourth quadrants to divide the core area in two, for intermediating operations of components constructing the memory device by generating internal command signals, internal address signals and control signals based on commands and addresses provided from outside;

a majority of ports located at edges of said each of the 4 quadrants, wherein respective ports perform independent communication with respective different target devices;

a first to a fourth global data bus, located in a row direction between the ports and the banks corresponding to said each of the 4 quadrants, for performing the parallel data transmission;

a first and a second global data bus connection means, located between two global data buses adjacent to each other in a row direction, for selectively connecting said two global data buses;

a multiplicity of local data buses, arranged in a column direction of each bank, for executing data transmission within the banks;

a plurality of local data bus connection means, located between two banks adjacent to each other in a column direction, for selectively connecting the local data buses corresponding to the two adjacent banks;

a plurality of bus connection means, located between each bank and a global data bus corresponding to a quadrant where said each bank is included, for performing data communication between each local data bus and said global data bus; and

a number of data transmission means, located between each port and a global data bus corresponding to said each port, for performing data transmitting/receiving between said each port and said global data bus.

6. The multi-port memory device as recited in claim 5, wherein each bank includes:

a plurality of memory cell arrays;

a multiplicity of bit-line sense amplifier arrays; and

a row decoder, wherein a unit page of each memory cell array is divided into 4 segments.

7. The multi-port memory device as recited in claim 5, wherein each of the ports includes:

a plurality of pads corresponding to data, addresses and

commands;

a pad buffer for buffering transmitting/receiving signals provided to the pads;

a decoder for decoding received data;

an encoder for encoding data to be transmitted; and

a data converter for converting received serial data to parallel data and parallel data to be transmitted to serial data.

8. The multi-port memory device as recited in claim 5, wherein each of the first and the second global data bus connection means includes interactive pipe registers as many as the number of lines of each of the first to the fourth global data buses.

9. The multi-port memory device as recited in claim 6, wherein each of the local data buses connects bit-line sense amplifiers of each bank and the bus connection means corresponding to said each bank and includes differential bus lines as many as the number of cells within a unit segment.

10. The multi-port memory device as recited in claim 9, wherein each of the local data bus connection means includes MOS transistors as many as the number of lines of a local data bus.

11. The multi-port memory device as recited in claim 9,

wherein each of the bus connection means includes transfer latches as many as the number of cells within the unit segment, each of the transfer latch containing:

a read sense amplifier for sensing and latching read data on the local data bus;

a read driver for providing the latched data to a global data bus of a quadrant where a corresponding bank is located;

a write latch for sensing and latching write data on the global data bus of the quadrant where the corresponding bank is located; and

a write driver for coupling write data to a local data bus of the corresponding bank.

12. The multi-port memory device as recited in claim 7, wherein each of the data transmission means includes:

a transmitter for providing write data coupled to a port connected to the data transmission means to a corresponding global data bus; and

a receiver for supplying read data provided from the corresponding global data bus to said port.

13. The multi-port memory device as recited in claim 5, further comprising:

voltage generators for producing an internal voltage based on an external voltage provided from outside; and

test logics located between ports corresponding to the first quadrant and the second quadrant and between ports

corresponding to the third quadrant and the fourth quadrant.